SONY

CXP402

CMOS 4-bit Single Chip Microcomputer

Description

The CXP402 is a CMOS 4-bit single chip microcomputer which consists of 4-bit CPU, ROM, RAM, 8-bit timer, 8-bit timer/counter, 18-bit time-base timer, LCD controller/driver, digital signal processor circuit for CD player, 1-bit DAC and the like.

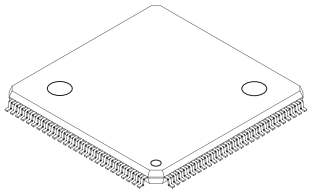
Features

- Instruction cycle 1.89µs for 16.93MHz oscillation
- ROM capacity 6144 × 8 bits
- RAM capacity 400 × 4 bits
  (Including stack and display area)
- LCD controller/driver (Enables to direct drive)
- 8-bit timer, 8-bit timer/event counter and 18-bit time-base timer are incorporated; they are independently controllable.
- Arithmetic and logical operations between the entire RAM area, I/O area and the accumulator by means of the memory mapped I/O.
- Entire ROM area can be referred by the table look-up instruction.

Digital Signal Processor (DSP) Block

- Playback mode supporting CAV (Constant Angular Velocity)
  - Frame jitter free
  - Allows relative rotational velocity readout
  - Supports spindle external control
- Wide capture range playback mode
  - Spindle rotational velocity following method
- 16K RAM
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- SEC strategy-based error correction
- Subcode demodulation and Sub Q data error detection
- Digital spindle servo
- 16-bit traverse counter
- Asymmetry correction circuit
- Servo auto sequencer
- Digital audio interface output
- Digital peak meter

112 pin LQFP (Plastic)



Digital Filter, DAC and Analog Low-Pass Filter Blocks

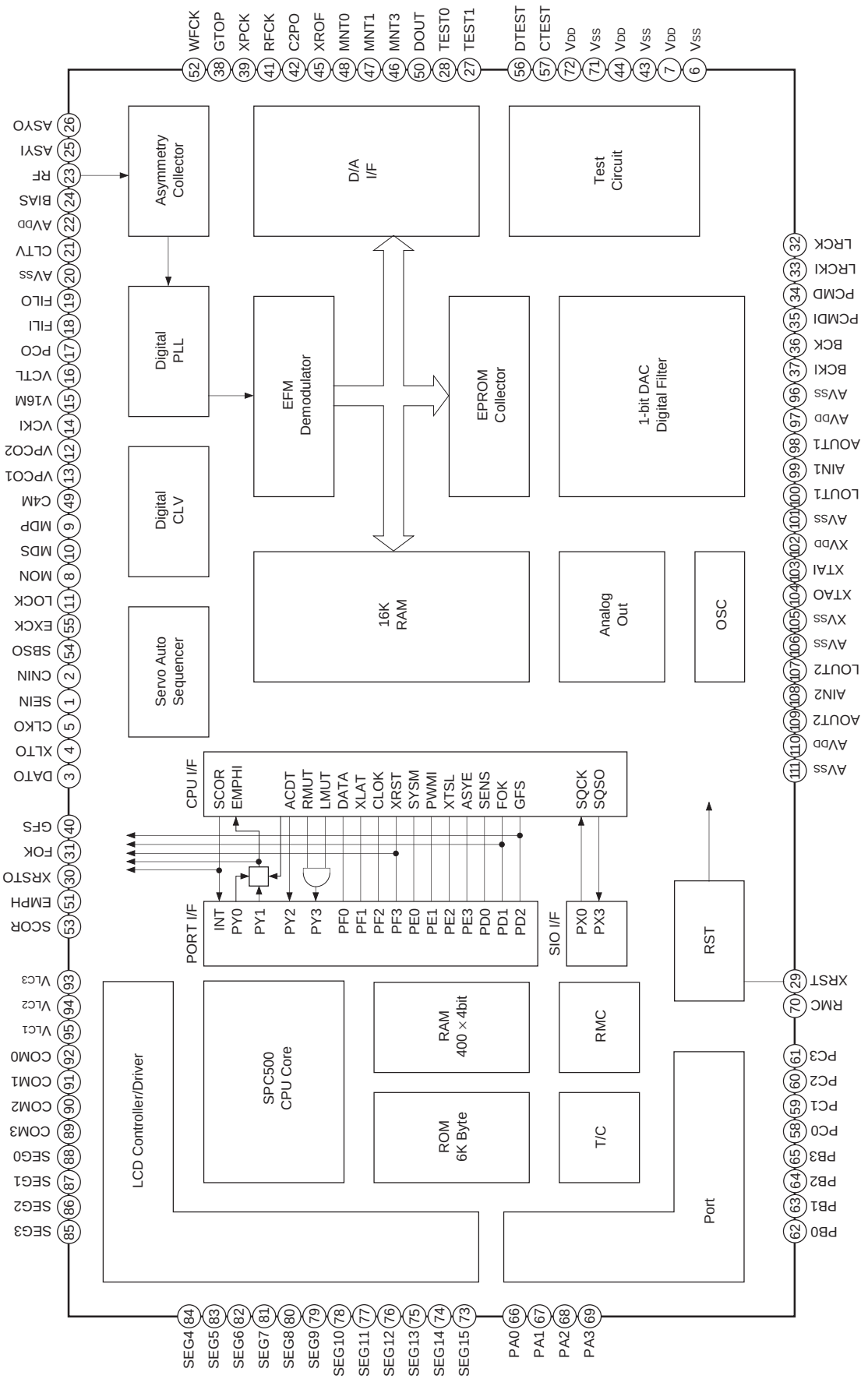
- DBB (digital bass boost) function
- Digital de-emphasis
- Digital attenuation
- Zero detection function
- 8Fs oversampling digital filter
- S/N: 100dB or more
  (master clock: 384Fs, typ.)
  Logical value: 109dB
- THD + N: 0.007% or less
  (master clock: 384Fs, typ.)
- Rejection band attenuation: –60dB or more
- 112-pin plastic LQFP
- Piggyback package (CXP401Z) available

Structure

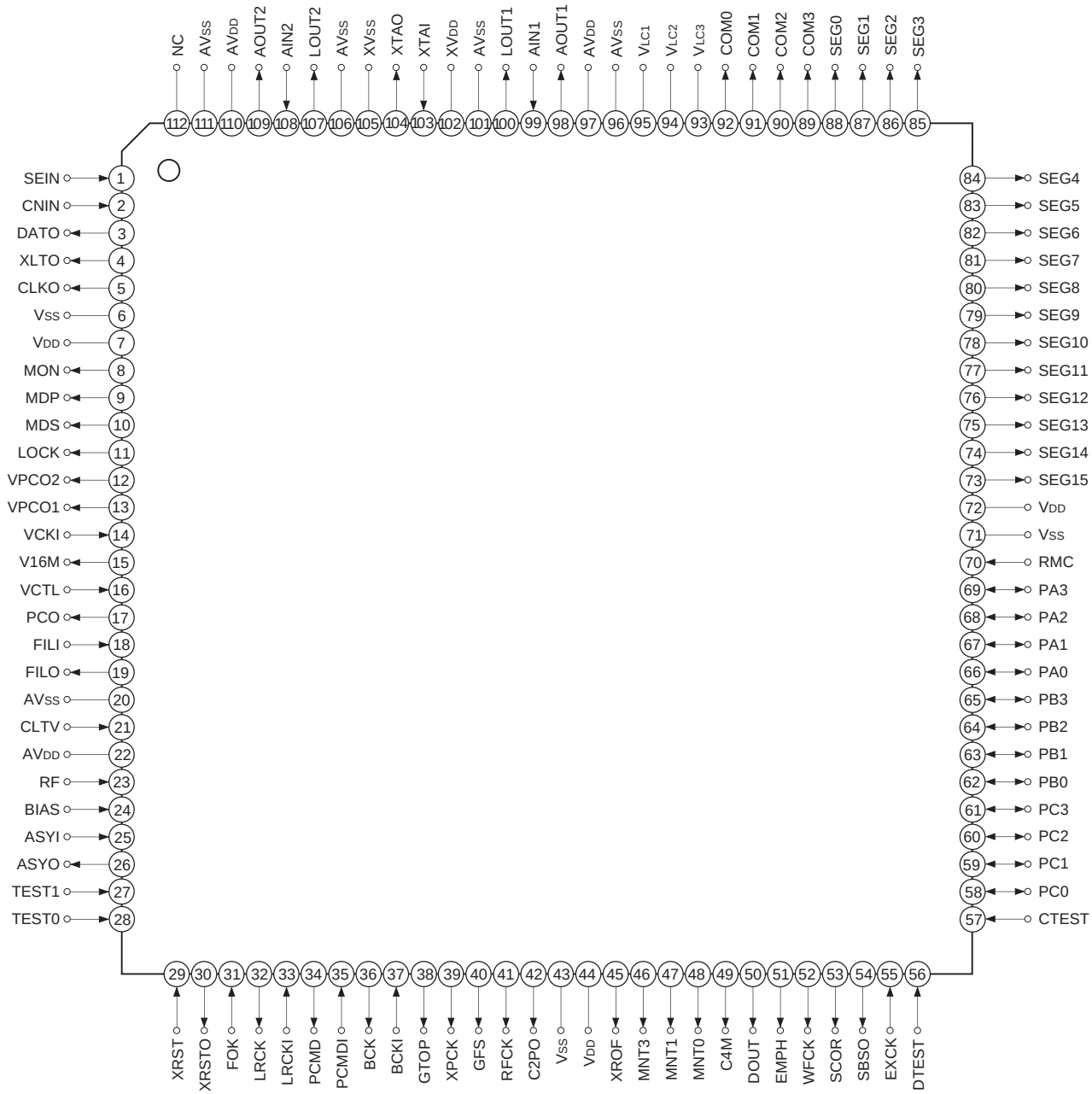
Silicon gate CMOS IC

E98924-PS

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	I/O	Description
PA0 to PA3	I/O	(Port A) 4-bit I/O port. I/O can be set in a unit of single bits. Pull-up resistor is attached for input. (4 pins)
PB0 to PB3	I/O	(Port B) 4-bit I/O port. I/O can be set in a unit of single bits. Pull-up resistor is attached for input. (4 pins)
PC0 to PC3	I/O	(Port C) 4-bit I/O port. I/O can be set in a unit of single bits. Pull-up resistor is attached for input. (4 pins)
SEG0 to SEG15	Output	LCD segment signal output. (16 pins)
COM0 to COM3	Output	LCD common signal output.
V_{LC1} to V_{LC3}		LCD bias power supply. Bias voltage is generated, which is 1/3 the supply voltage due to the internal resistor. (3 pins)
SEIN	Input	SENS input from SSP.
CNIN	Input	Track jump count signal input.
DATO	Output	Serial data output to SSP.
XLTO	Output	Serial data latch output to SSP.
CLKO	Output	Serial clock output to SSP.
MON	Output	Spindle motor ON/OFF control output.
MDP MDS	Output (tri-state)	Spindle motor servo control. (2 pins)
LOCK	Output	Lock signal output. GFS is sampled at 460Hz and; when GFS is high, this pin outputs a high signal. If GFS is low eight convective samples, this pin outputs low.
VPCO1 VPCO2	Output (tri-state)	Wide-band EFM PLL charge pump output. (2 pins)
VCKI	Input	Wide-band EFM PLL VCO2 oscillation input.
V16M	Output	Wide-band EFM PLL VCO2 oscillation output.
VCTL	Input	Wide-band EFM PLL VCO2 control voltage input.
PCO	Output (tri-state)	Master PLL charge pump output.
FILI	Input	Master PLL filter input.
FILO	Output (Analog)	Master PLL filter output.
CLTV	Input	Master VCO control voltage input.
RF	Input	EFM signal input.
BIAS	Input	Asymmetry circuit constant current input.
ASYI	Input	Asymmetry comparator voltage input.
ASYO	Output	EFM output. (full swing)
XRST	Input	System reset input. Active at low.

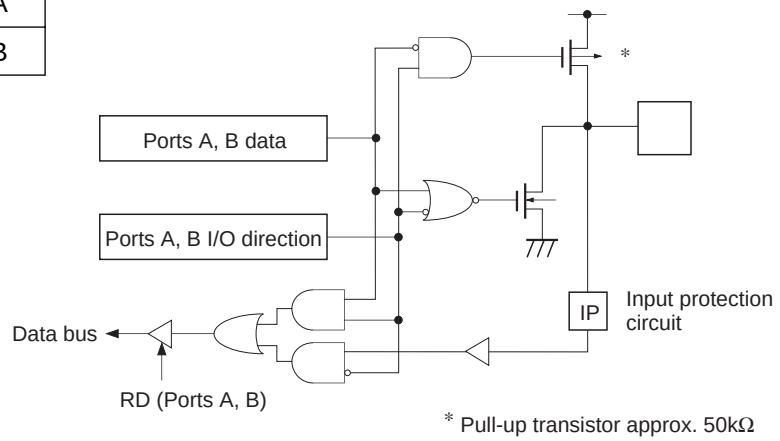
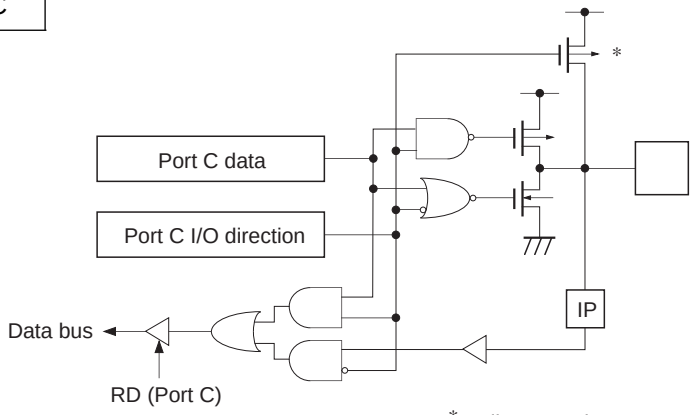
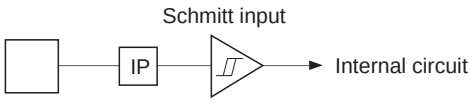
Symbol	I/O	Description
XRSTO	Output	Reset signal output. Active at low.
FOK	Input	Focus OK input. Used for SENS output and servo auto sequencer.
LRCK	Output	D/A interface LR clock output. (f = Fs)
LRCKI	Input	LR clock input.
PCMD	Output	D/A interface serial data output.
PCMDI	Input	D/A interface serial data input.
BCK	Output	D/A interface bit clock output.
BCKI	Input	D/A interface bit clock input.
GTOP	Output	GTOP output.
XPCK	Output	XPLCK output.
GFS	Output	GFS output.
RFCK	Output	RFCK output.
C2PO	Output	C2PO output.
XROF	Output	XRAOF output.
MNT3	Output	MNT3 output.
MNT1	Output	MNT1 output.
MNT0	Output	MNT0 output.
C4M	Output	1/4 frequency division output of the oscillation input. (4.2336MHz for 16.3944MHz)
DOUT	Output	Digital Out output.
EMPH	Output	De-emphasis ON/OFF output. High is output for ON; low is output for OFF.
WFCK	Output	WFCK output.
SCOR	Output	Subcode sync detection output. Outputs a high signal when either subcode sync S0 or S1 is detected.
SBSO	Output	Sub P to W serial data output.
EXCK	Input	SBSO serial clock input.
AOUT1	Output (Analog)	Lch analog output.
AIN1	Input (Analog)	Lch operational amplifier input.
LOUT1	Output	Lch LINE output.
AOUT2	Output (Analog)	Rch analog output.
AIN2	Input (Analog)	Rch operational amplifier
LOUT2	Output	Rch LINE output.
RMC	Input	Remote control receiver circuit input.
XTAI	Input	Connect a crystal for system clock oscillation. When the clock is supplied externally, input it to the XTAI pin and leave the XTAO pin open.
XTAO		
NC		No connected.

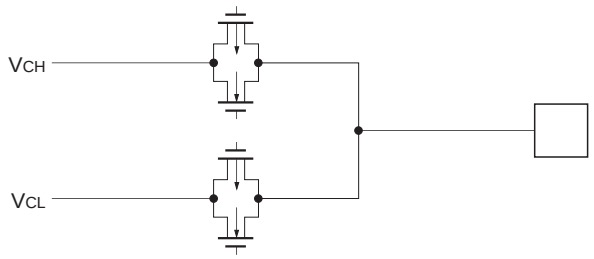
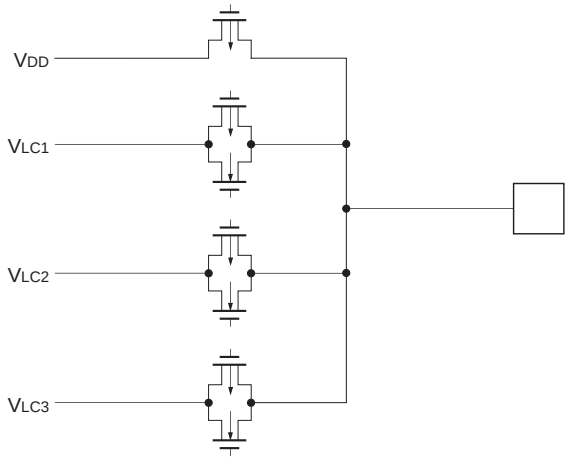
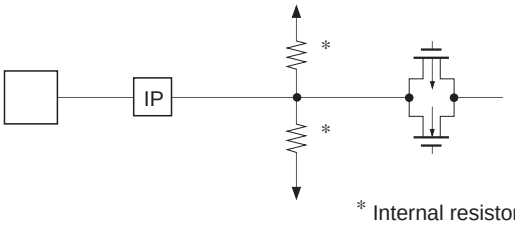
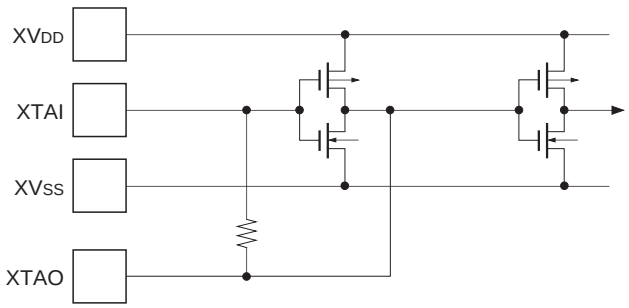
Symbol	I/O	Description
V_{DD}		Positive power supply.
V_{SS}		GND.
AV_{DD}		Positive power supply for analog circuit.
AV_{SS}		GND for analog circuit.
XV_{DD}		Positive power supply for oscillation circuit.
XV_{SS}		GND for oscillation circuit.
TEST1	Input	Test for LSI. Connect to GND for normal operation.
TEST0	Input	
DTEST	Input	
CTEST	Input	

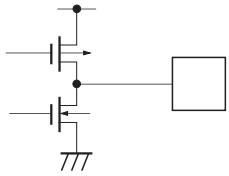
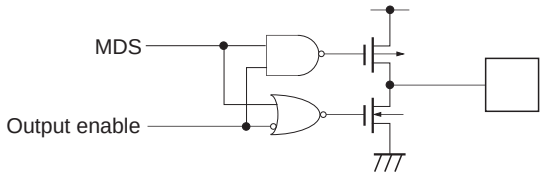
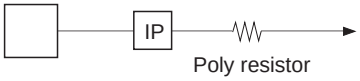
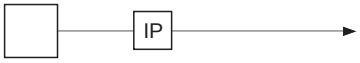
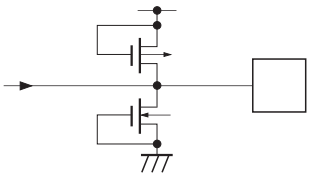
Notes

- Power supply pins AV_{DD}, AVss, XV_{DD}, XVss, V_{DD} and Vss should process all the pins.
- PCMD is the MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window open.)
- XUGF is the frame sync obtained from the EFM signal, and is negative pulse. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- The GFS signal goes high when the frame sync and the insertion timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136µs (at normal speed).
- C2PO represents the data error status.
- XRAOF is generated when the 16K RAM exceeds the ±4F jitter margin.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0 to PA3 PB0 to PB3 8 pins	Port A Port B  * Pull-up transistor approx. 50kΩ	Hi-Z
PC0 to PC3 4 pins	Port C  * Pull-up transistor approx. 50kΩ	Hi-Z
RMC XRST SEIN CNIN VCKI FOK LRCKI PCMDI BCKI EXCK 10 pins	 * EMPHI is not Schmitt input.	Hi-Z

Pin	Circuit format	When reset
SEG0 to SEG15 16 pins		VDD level
COM0 COM1 COM2 COM3 4 pins		VDD level
VLC1 VLC2 VLC3 3 pins	 * Internal resistor approx. 20kΩ	VLC1 = 3/4VDD VLC2 = 2/4VDD VLC3 = 1/4VDD (when pins left open)
XVDD XTAI XTAO XVSS 4 pins		Oscillation

Pin	Circuit format	When reset
PCO MDP VPCO1 VPCO2 4 pins		—
MDS 1 pin		—
VCTL FILI CLTV RF BIAS ASYI 6 pins		—
AIN1 AIN2 2 pins		—
AOUT1 AOUT2 LOUT1 LOUT2 4 pins		—

Pin	Circuit format	When reset
DATO XLTO CLKO LOCK MON V16M FILO ASYO XRSTO LRCK PCMD BCK GTOP XPCK GFS RFCK C2PO XROF MNT3 MNT1 MNT0 C4M DOUT EMPH WFCK SCOR SBSO 27 pins		—

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0*1	V	
LCD bias voltage	V_{LC1}, V_{LC2}, V_{LC3}	–0.3 to +7.0*2	V	
Input voltage	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
High level output current	I_{OH}	–5	mA	Output pin (value per pin)
High level total output current	$\sum I_{OH}$	–70	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Output pin (value per pin)
Low level total output current	$\sum I_{OL}$	100	mA	Total of output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–40 to +125	°C	
Allowable power dissipation	P_D	600	mW	

*1 The potential difference between analog power supplies AV_{DD}, AVss, the oscillation power supplies XV_{DD}, XVss and V_{DD}, Vss should be within ±0.3V.

*2 V_{LC1}, V_{LC2}, V_{LC3}, V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operation Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	3.4	5.25	V	Operation guaranteed range
LCD bias voltage	V_{LC1}, V_{LC2}, V_{LC3}	Vss	V_{DD}	V	Liquid crystal power supply range*1
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*2
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*2
Analog input voltage	V_{IA}	0	V_{DD}	V	*3
Operating temperature	Topr	–20	+75	°C	

*1 The optimal value depends on the characteristics of the used LCD element. Also, the LCD bias voltage is biased to 1/3 the supply voltage by the resistor of approximately 20kΩ in the LSI.

*2 RME, XRST, EXCK, FOK, SEIN, CNIN, VCKI, LRCKI, BCKI, PCMDI pins

*3 CLTV, FILI, RF, VCTL, AIN1, AIN2, BAIS, ASYI pins

Electrical Characteristics

DC characteristics (Topr = –20 to +75°C, V_{SS} = AV_{SS} = XV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA, PB	V_{DD} = 4.75V, I_{OH} = –0.1mA	4.25			V
		BCKI, C2PO, SBSO, DATO, XLTO, CLKO, PA (V_{OL} only), PB (V_{OL} only), PC, MON, MDS, LOCK, LRCK, PCMD, BCK, GTOP, GFS, RFCK, XROF, MNT3, MNT1, MNT0, DOUT, WFCK, SCOR, MDP, VPCO2, VPCO1, PCO, V16M, EMPH, XPCK, ASYO, C4M, XRSTO, LRCK, PCMD	V_{DD} = 4.75V, I_{OH} = –2.0mA	4.25			V
		FILO	V_{DD} = 4.75V, I_{OH} = –0.28mA	4.25			V
Low level output voltage	V_{OL}		V_{DD} = 4.75V, I_{OL} = 0.36mA			0.4	V
			V_{DD} = 4.75V, I_{OL} = 6.0mA			0.4	V
			V_{DD} = 4.75V, I_{OL} = 9.0mA			0.6	V
Input current	I_{IH}	XTAI	V_{DD} = 5.25V, V_{IH} = 5.25V	0.2		30	µA
	I_{ILE}	XTAI	V_{DD} = 5.25V, V_{IL} = 0.4V	–0.2		–30	µA
	I_{IL}	PA to PC	V_{DD} = 5.25V, V_{IL} = 0.4V	–0.06		–0.2	mA
High-impedance I/O leak current	I_{IZ}	PCMDI, RME, XRST, EXCK, FOK, SEIN, CNIN, VCKI, LRCKI, BCKI, CLTV, FILI, RF, VCTL, AIN1, AIN2, MDP, MDS, VPCO1, VPCO2	V_{DD} = 5.25V V_I = 0, 5.25V			±5	µA
LCD bias voltage resistance	R_B	V_{LC1}, V_{LC2}, V_{LC3}	V_{DD} = 5V, V_{LC1}, V_{LC2}, V_{LC3} pins left open	7		30	kΩ
Common output impedance	R_{COM}	COM0 to COM3	V_{DD} = 5.0V V_{LC1} = 3.75V V_{LC2} = 2.5V V_{LC3} = 1.25V		3	5	kΩ
Segment output impedance	R_{SEG}	SEG0 to SEG15			5	15	kΩ
Supply current	I_{DD}	V_{DD}, AV_{DD}	V_{DD} = 5.25V 16.93MHz self-excited oscillation operation All output pins left open		37	80	mA
Input capacity	C_{IN}	Pins other than V_{LC1} to V_{LC3}, COM0 to COM3, SEG0 to SEG15, PA to PC, V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, XV_{DD}, XV_{SS}	Clock 1MHz 0V for no-measured pins		10	20	pF

AC Characteristics

1. XTAI pin

(1) When using self-excited oscillation

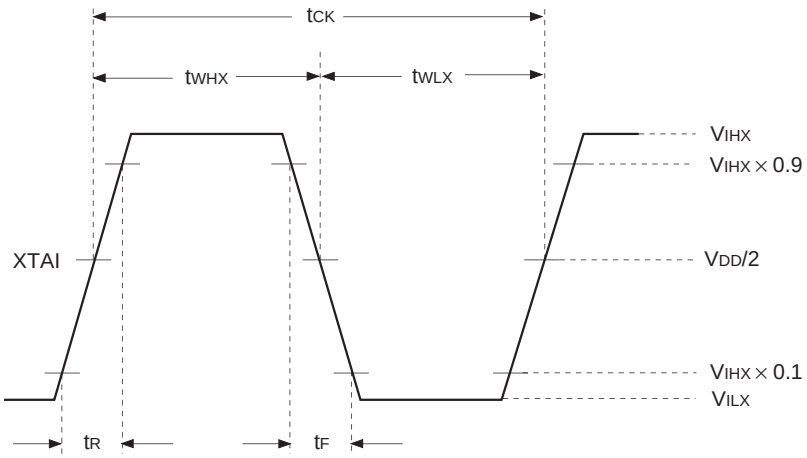
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 5%)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	15	16.93	20	MHz

(2) When inputting pulses to XTAI pin

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 5%)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CK}	26		1,000	ns
Input high level	V_{IHX}	V_{DD} – 1.0			V
Input low level	V_{ILX}			0.8	V
Rise time, fall time	t_R, t_F			10	ns



(3) When inputting sine waves to XTAI pin via a capacitor

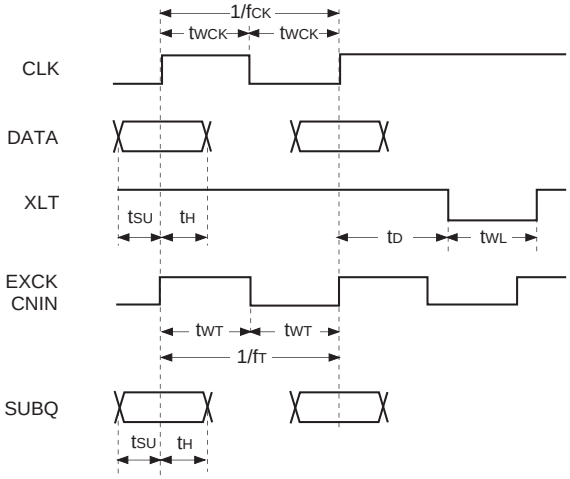
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 5%)

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD} + 0.3	Vp-p

2. CNIN, EXCK pins

(V_{DD} = AV_{DD} = 5.0V ± 5%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

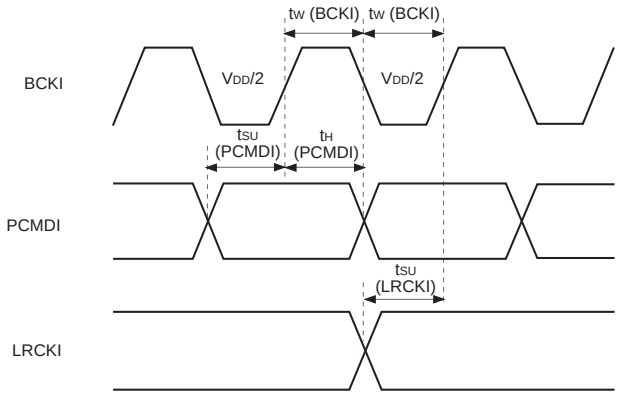
Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK frequency	f_T			0.65	MHz
EXCK pulse width	f_{WT}	750			ns



3. BCKI, LRCKI, PCMDI pins

(V_{DD} = AV_{DD} = 5.0V ± 5%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
BCK pulse width	t_W		94			ns
DATAL, R setup time	t_{SU}		18			ns
DATAL, R hold time	t_H		18			ns
LRCK setup time	t_{SU}		18			ns



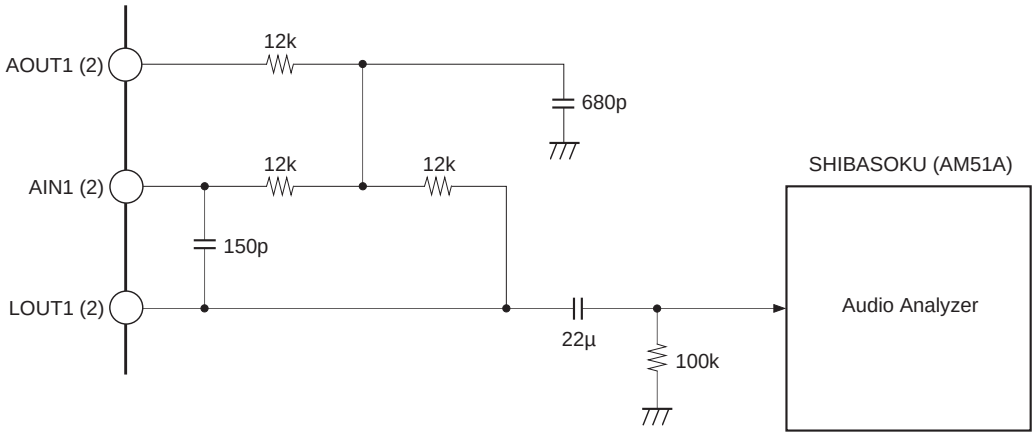
1-bit DAC, LPF Blocks Analog Characteristics

Analog characteristics (V_{DD} = AV_{DD} = 5.0V, V_{SS} = AV_{SS} = 0V, Ta = 25°C)

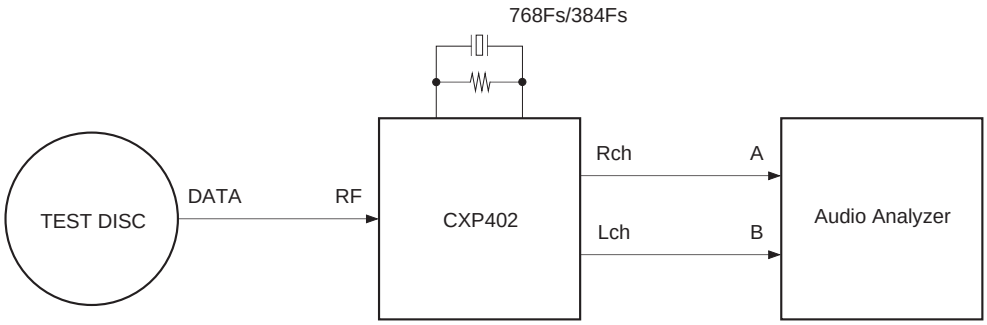
Item	Symbol	Conditions	Crystal	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD	1kHz, 0dB data	384Fs		0.0050	0.0070	%
			768Fs		0.0045	0.0065	
Signal-to-noise ratio	S/N	1kHz, 0dB data (A-filter)	384Fs	96	100		dB
			768Fs	96	100		

Fs = 44.1kHz.

The total harmonic distortion and signal-to-noise ratio are measured by the circuits shown below.



LPF external circuit diagram



Block diagram of analog characteristics measurement

(V_{DD} = AV_{DD} = 5.0V, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Applicable pins
Output voltage	V_{OUT}		1.23*		Vrms	*1
Load resistance	R_L	8			kΩ	*1

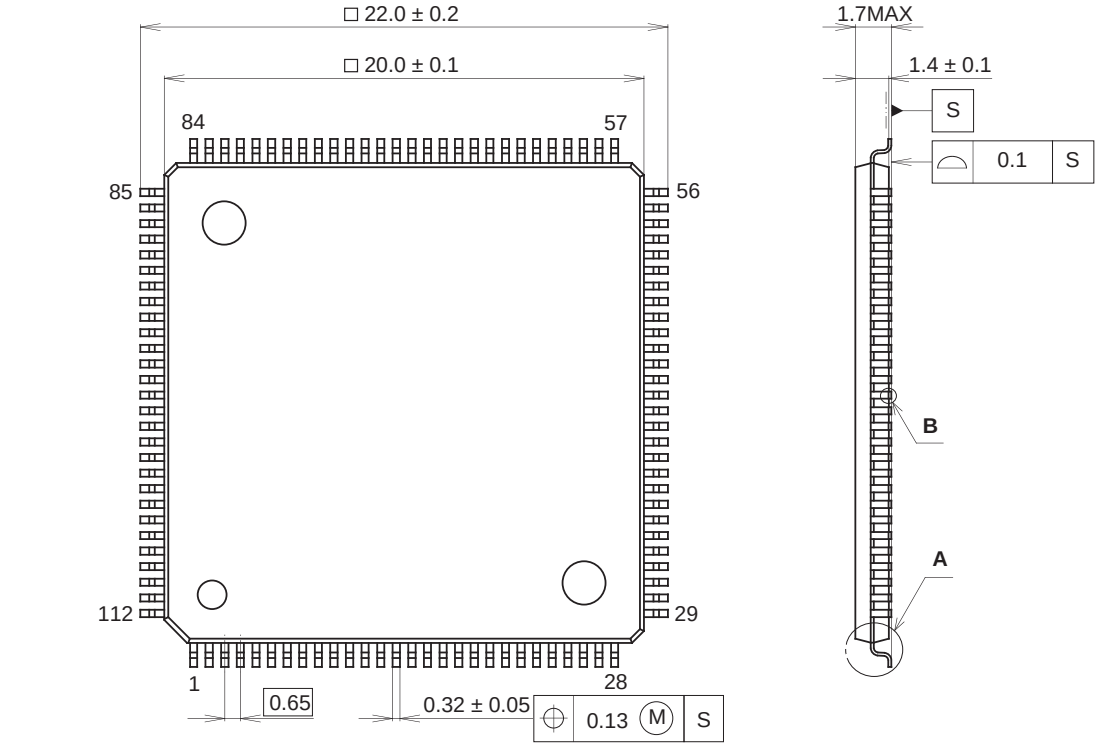
* When a sine wave of 1kHz, 0dB is output.

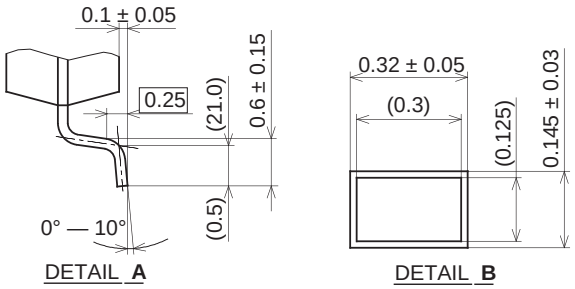
Applicable pins

*1 LOUT1, LOUT2

Package Outline Unit: mm

112PIN LQFP(PLASTIC)





SONY CODE	LQFP-112P-L01
EIAJ CODE	LQFP112-P-2020
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	1.3g